UniPro v3.0 FPGA IP Core

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Overview

MIPI® compliant UniPro® v3.0 IP core for reuse in Universal Flash Storage hosts, devices or platforms. The IP core can be used for FPGA or ASIC implementations. The architecture is fully optimized for FPGA implementations and focuses on the UniPro feature set mandated for use in JEDEC UFS 5.0 applications.

The IP core is parameterizable and can be customized for system requirements or customer specific demands. The core includes comprehensive documentation, including architectural specification, Register Description files in SystemRDL, scripts and log files and a bring up testbench written in UVM.

The design has been developed in RTL following the latest SystemVerilog P1800-2017 standard and is delivered as unencrypted source code. It has been designed under a state-of-the-art Synopsys design flow and has been verified on Vivado® 2025.2 Versal™ devices.

The IP Core supports flexible license models. Depending on the selected license model, the core is delivered with comprehensive integration and customization support. Additionally, on-site training is offered to allow engineering staff to quickly acquire full ownership of the RTL code.

The UniPro® v3.0 IP Core is in production.

Key Features

General

- Optimized for JEDEC UFS 5.0
- MIPI® M-PHY® 6.0 HS-G6A/B support
- Backward compatible to UniPro® v2.0
- Architecture suitable for FPGA (Altera / Xilinx)
  ~90 Gbps throughput Agilex™ / Versal™
- MIPI® CPort data interface 256-bit wide
- MIPI® DME interface 32-bit AXI-4-Lite
- MIPI® RMMI interface 128-bit per Lane
- Internal Data Processing:
  - 32 bytes per clock @ 375MHz
- Additional diagnostics registers for debug
- SystemVerilog 2018, SystemRDL 2.0 and UVM 1.2 code base

Transport Layer L4, optimized for UFS 5.0

- local CPort #0 support
- CSV: compliant with UFS 5.0
- L4 test feature

Network Layer L3

- Header handling

Data Link Layer L2

- Support for credit sizes 32 and 128
- TCO Support Only
- 2x 16KByte two-port RAM, single clock

PHY Adapter Layer L1.5

- Up to 2 M-PHY® Lanes
- Supports ResetMode = HS_MODE/LS_MODE
- 1b1b TFS Frame coding and 8b10b LineCoding
- Novel 1b1b error counters
- Novel QoS measurement for 1b1b Link
- CRC64, RS (255,3) error detection and correction
- Support for built-in M-PHY v6.0 test

MPHY Layer

- RDL description of all MPHY registers
- SystemVerilog example code provided

Device Management Entity (DME)

- AMBA® AIX04 Lite CPU Slave Interface
- Quality of Service Measurements
- Debug status registers and failure interrupts
- Request, confirmations and indications accessible via software or hardware.

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Block Diagram

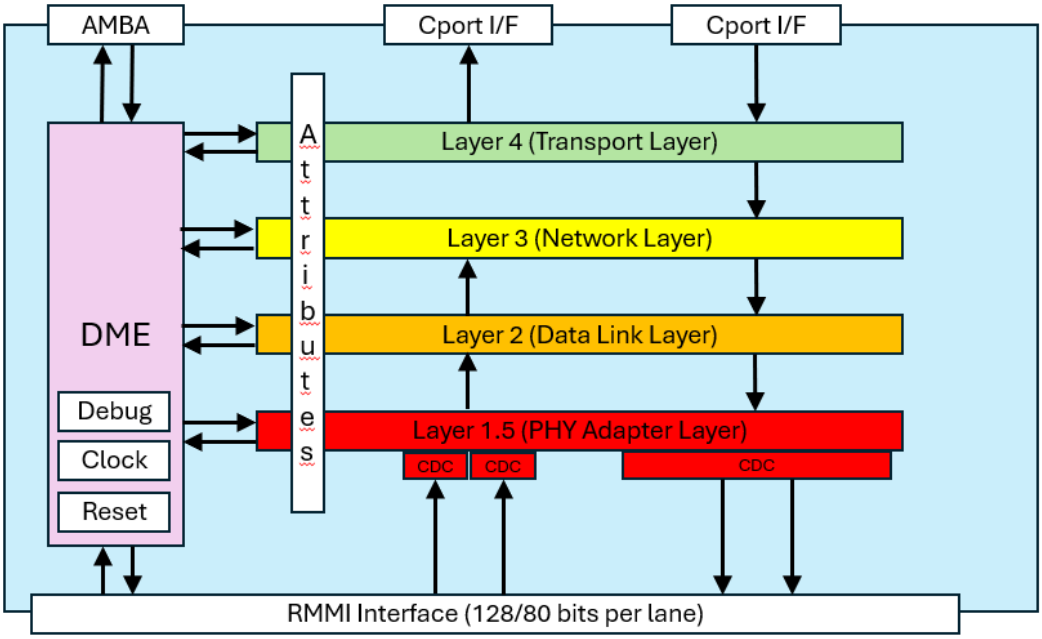

Figure 1 - UniPro 3.0 IP Block Diagram

Deliverables

- IP- Functional Specification,
- IP- Architectural Specification
- Encrypted or Unencrypted RTL SystemVerilog P1800-2017 code
- SystemRDL v2.0 Register Description
- Lint Logs
- Synthesis scripts
- STA constraints
- STA log files
- Bring up testbench
- Verification execution proof, documents, coverage logs

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Core Resources

Xilinx Versal resource usage summary.

Name	Registers (3507968)	CLB LUTs (1753984)	LUT as Logic (1753984)	LUT as Memory (876992)	LOOKAHEAD8 (219248)	SLICE (219248)	CLB Registers (3507968)	Block RAM Tile (2541)
i_unipro (unipro)	82631	120255	114541	5714	270	22845	82631	38.5
i_dme (dme)	6008	5328	5328	0	97	1200	6008	0
i_l2_wrap (l2_wrap)	35226	59345	55840	3505	81	10895	35226	37.5
i_l3_wrap (l3_wrap)	1192	104	104	0	6	234	1192	0
i_l4_wrap (l4_wrap)	5154	8036	8036	0	44	1742	5154	0
i_l15_wrap (l15_wrap)	34804	47420	45211	2209	42	9473	34804	1
i_reset_ctrl (reset_ctrl)	237	17	17	0	0	137	237	0

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