PROTOCOL INSIGHT

HS-G5 Interposer (FG5AMPGR) – Rev B

Quick Start / User Guide

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Contents

Introduction

The HS-G5 Interposer board, FG5AMPGR, allows developers to tap signals between the Host and DUT and send them to a protocol analyzer using SMP-mini connectors. The UFS device is placed directly on the interposer board in a grypper socket. The interposer can be soldered directly into the customer system, or you can use a dual grypper socket connection. More information on grypper sockets can be found on their website.

The grypper board uses a 66 / 33 resistive divider and provides the "66" side to the Host / DUT. This provides an additional ~ 2 dB of signal for the Host / DUT, compared to a 50 / 50 resistive divider. The "33" side is then amplified and sent to the protocol analyzer. The amplification settings are adjustable.

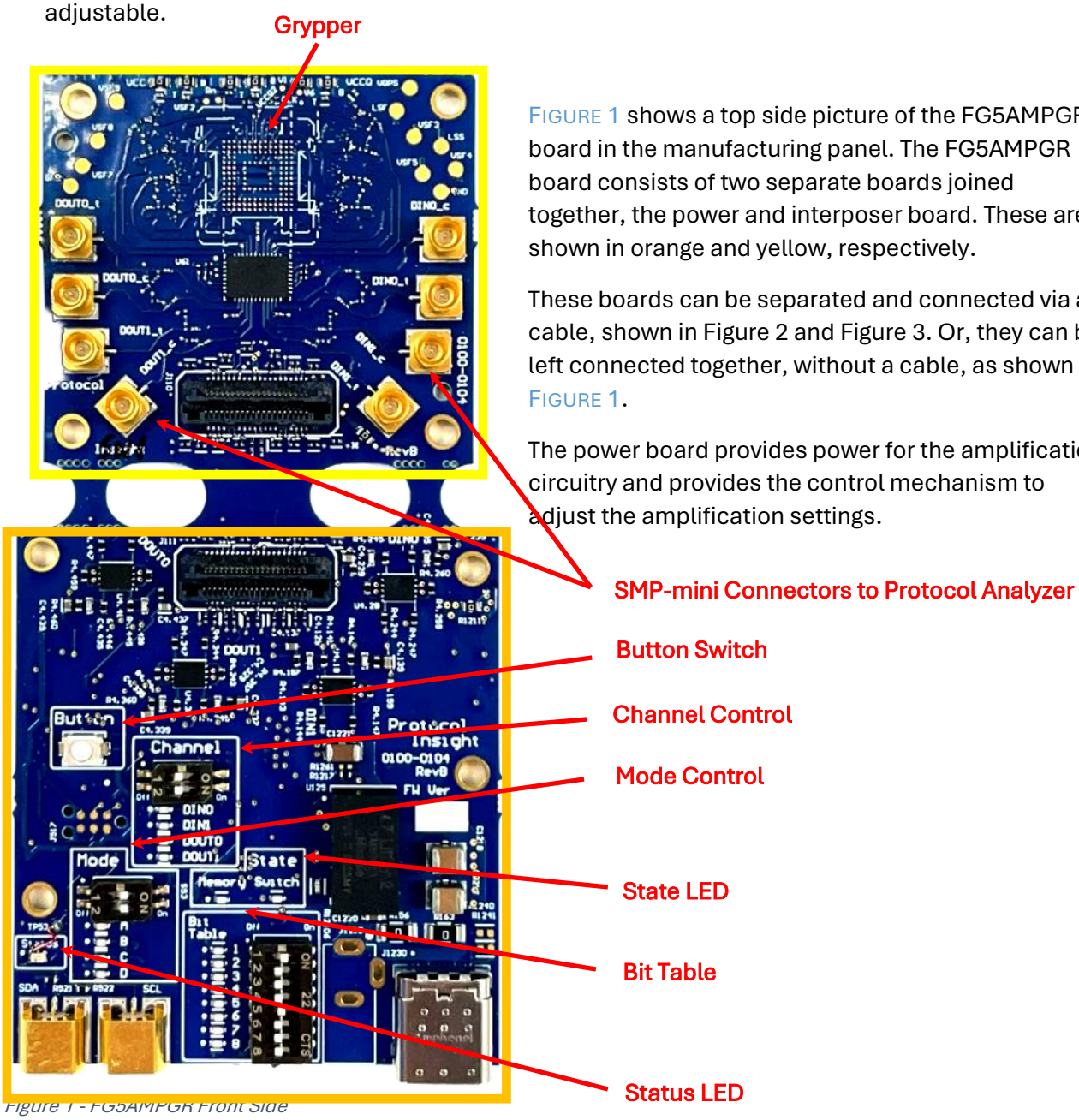


Figure 1 - FG5AMPGR Front Side

FIGURE 1 shows a top side picture of the FG5AMPGR board in the manufacturing panel. The FG5AMPGR board consists of two separate boards joined together, the power and interposer board. These are shown in orange and yellow, respectively.

These boards can be separated and connected via a cable, shown in Figure 2 and Figure 3. Or, they can be left connected together, without a cable, as shown in FIGURE 1.

The power board provides power for the amplification circuitry and provides the control mechanism to adjust the amplification settings.

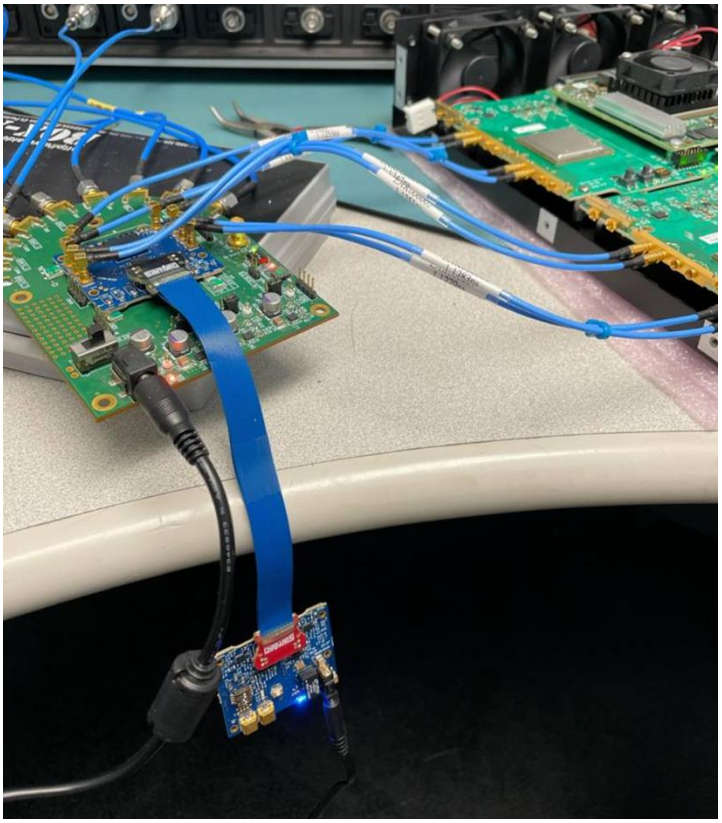


Figure 2 - FG5AMPGR Lab Use Case

FIGURE 2 shows a picture of the FG5AMPGR board being used in a lab environment. The power and interposer board are connected via a blue Samtec ribbon cable. The protocol analyzer is connected to the interposer board with SMP-mini to SMP cables. In FIGURE 2 the protocol analyzer is on the right-hand side of the picture. The UFS carrier board, which is a test platform, is underneath the interposer board. The grypper socket on the bottom side of the interposer board attaches to the balls on the carrier board. The UFS device is connected to the interposer board via the grypper socket on the top side of the interposer board.

FIGURE 3 shows the top-side view of the FG5AMPGR interposer and power board connected with a ribbon cable. The grypper socket is soldered down to the top of the interposer board on the left side of the picture. A UFS device can be pressed into the socket and the grypper will grip onto the solder balls of the UFS device.

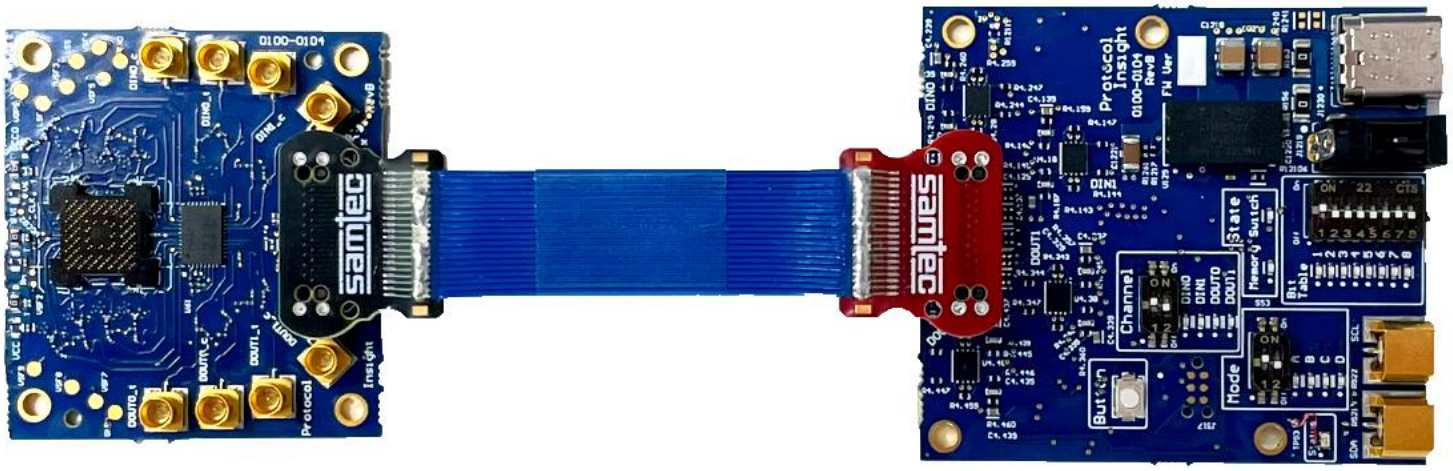


Figure 3 - Interposer and Power Board with Ribbon Cable (top side view)

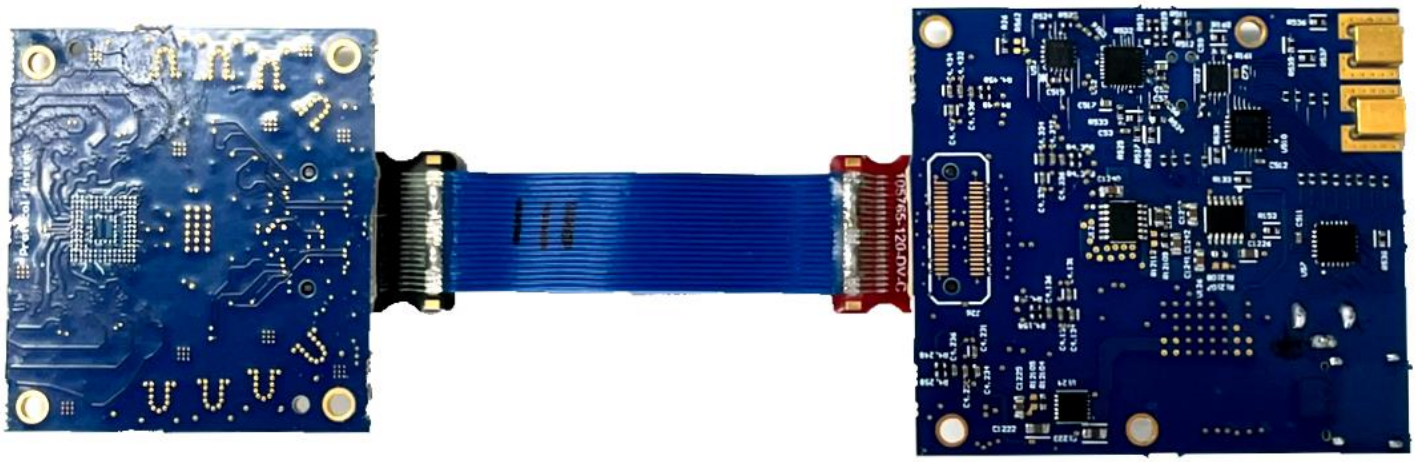


Figure 3 - Interposer and Power Board with Ribbon Cable (bottom side view)

FIGURE 4 shows the bottom side view of the FG5AMPGR. A socket is not currently attached to the bottom side of the interposer board. To connect this board to a test target there are several options:

- It can be soldered directly to a board.
- An elastomer can be soldered to the interposer and target board. The elastomer increases the z-height and may be useful in some environments.
- Another grypper socket can be soldered directly to the bottom of the interposer. The grypper socket provides some z-height clearance and can be push connected to the target board. The grypper attaches to the solder balls on the target board.

FIGURE 4 shows a diagram illustrating the use of two grypper sockets attached to the interposer board. The target board is shown in green, the interposer board is blue, and the grypper sockets are in black. In this configuration the grypper sockets are soldered directly to the interposer board and target board (balls shown in green). The grypper sockets attach to the interposer board and the UFS device by gripping the solder balls. This is depicted on the right side of FIGURE 4.

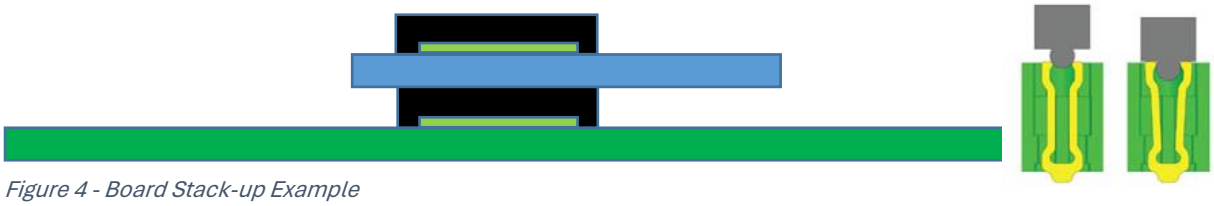


Figure 4 - Board Stack-up Example

Use Case Requirements

The interposer board requires the following minimum differential signal requirements. If an oscilloscope is available, you can confirm your test configuration aligns with these parameters, shown in FIGURE 5.

- Inner eye width = 100ps Minimum for GEAR3, 60ps for GEAR4 and 30ps for GEAR5.
- Inner eye height = 90 mVpp Minimum.
- Eye Amplitude = 620 mV.
- Maximum differential signal amplitude 620 mVpp.

FIGURE 5 shows the EYE diagram requirements at the connection point.

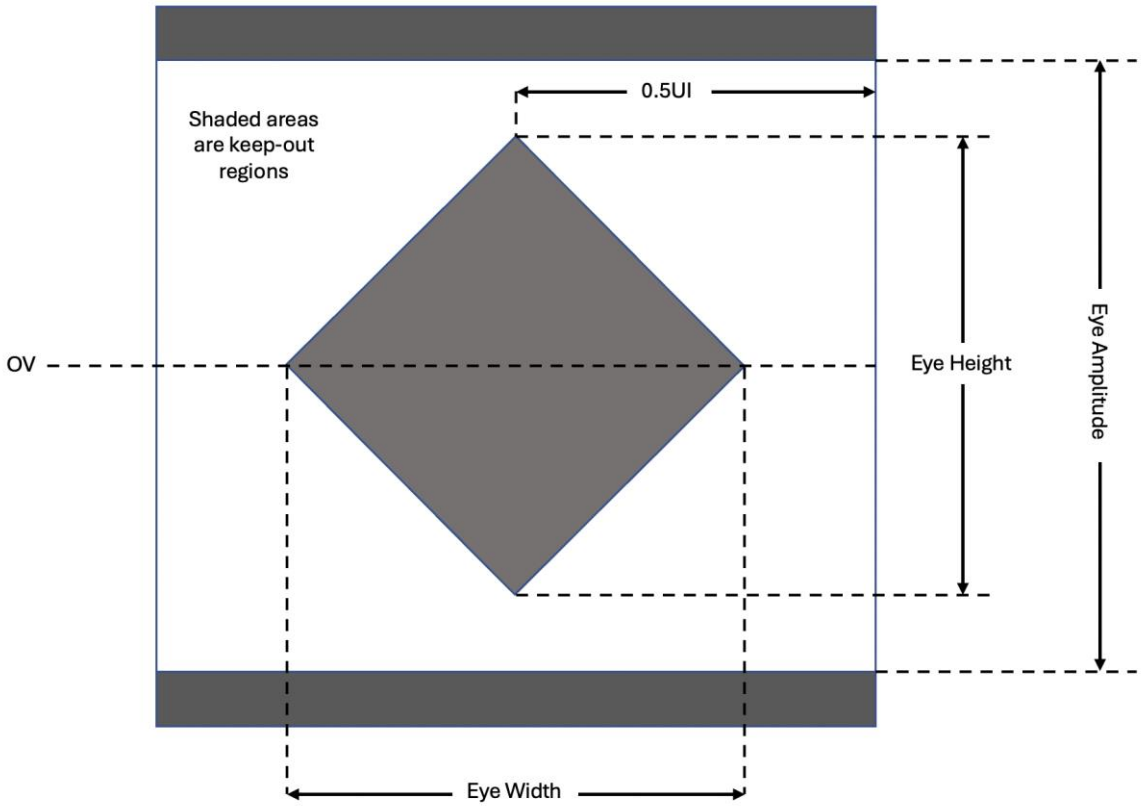


Figure 5 - EYE Diagram

Connecting the Interposer Board to the Protocol Analyzer

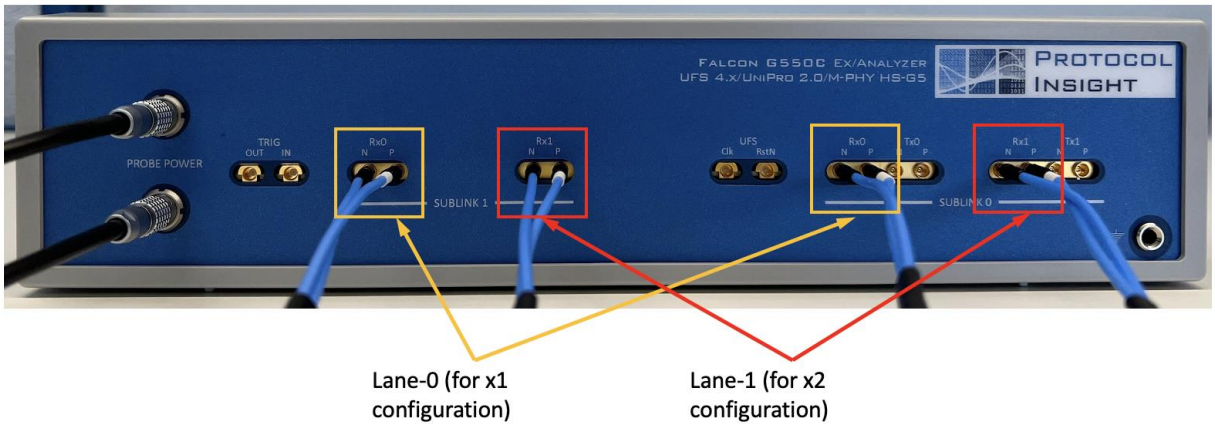


Figure 6 - Cabling Between Interposer and Analyzer

Cable Configuration

When connecting the DUT, ensure you use low-loss, phase matched cables. The connectors on the interposer board, FG5AMPGR, are male SMP-mini. The connectors on the protocol analyzer are male SMP. Below are the cable characteristics we recommend:

- Low-loss material, < 1 dB per foot of insertion loss @ 12 GHz
- Limit the length of the cables to < 12-inches in length
- The cables must be 50 ohm and phase-matched
- Right angle SMP-mini cable to ease escapement from board

Match the P/N connections when connecting the cables (P to P, N to N). The nomenclature of JESD220B is adopted on the board, T (true) is P and C (complement) is N. The recommended cable, FG5AMPSP-C, is a 12-inch phase matched SMP female (protocol analyzer side) to a right angle SMP-mini female (amp splitter side). We strongly recommend using a cable extraction tool to avoid damaging the connectors or cables.

Recommended Connection for a x1 Configuration

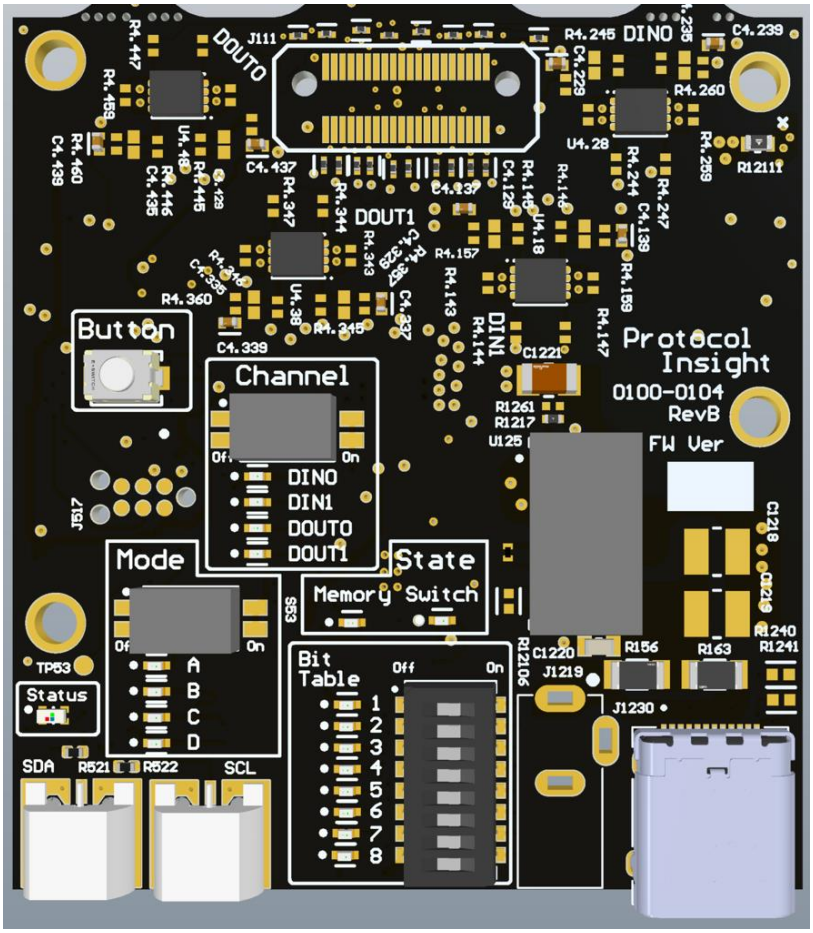
In a x1 configuration we expect a host and device single lane configuration. Use two matched pairs of SMP-mini to SMP cables to connect the DIN0 and DOUT0 to the protocol analyzer Sublink 0 Rx0 or Sublink 1 Rx0, respectively. Lane 0 from the host and device must connect to Rx0 on the PA.

Recommended Connection for a x2 Configuration

In a x2 configuration we expect a host and device dual lane configuration. Use four matched pairs of SMP-mini to SMP cables to connect the DOUT (0 and 1) and DIN (0 and 1) to the protocol analyzer, Sublink 0 Rx0 and Rx1 and Sublink 1 Rx0 and Rx1. **Example:** DIN0 and DIN1 should be connected to Sublink 0 Rx0 and Rx1, respectively. DOUT0 and DOUT1 should be connected to Sublink 1 Rx0 and Rx1, respectively.

Controls and Status

There are six different sets of controls and status LEDs on the interposer STATUS, MODE, CHANNEL, STATE, BUTTON and BIT TABLE.



Power

The interposer is powered by +5V DC via a USB-C power cable. The interposer is not a USB-C compatible device. A USB-A AC/DC adapter and a USB-A to USB-C cable, are recommended.

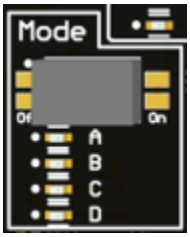
Status

The status light can be red, green or blue.

- Red indicates an error.
- Green is the normal operating color.
- Blue indicates offset calibration is running.

If the red status light is illuminated, power cycle the unit by removing and then reinserting the USB-C power cable.

Mode



There are four primary modes of operation: MODE A, MODE B, MODE C and MODE D. The Mode switch bank controls which mode is currently enabled. A bit is set low when the switch is toggled to the left side and set high when toggled to the right side.

Mode A

Mode Switch = '00' : MODE A selects all four channels in a broadcast mode configuration, indicated by the illumination of the Mode A LED and all four CHANNEL LEDs. Any changes to the BIT TABLE switch will be automatically applied to all four channels and written to non-volatile memory, indicated by three blinks on the Memory LED. To change channel settings individually you should use MODE B.

☞ If the Mode Switch is toggled to MODE A (from B or C), the currently saved MODE B DIN0 values will be written to all channels. To change the programmed value, simply toggle the BIT TABLE switch to the desired setting.

Mode B

Mode Switch = '01' : MODE B enables individual channel control. In MODE B, the Mode B LED and selected channel LED will be illuminated. Any changes to the BIT TABLE switch will be automatically applied to the selected channel and written to non-volatile memory, indicated by three blinks on the Memory LED. When a different channel is selected on the CHANNEL switch, the current non-volatile memory settings will be applied to the selected channel. To change the channel value simply toggle the BIT TABLE switch to the desired setting. This setting will be applied and written to non-volatile memory, indicated by three blinks on the STATE Memory LED.

Mode C

Mode Switch = '10': MODE C enables offset calibration. In Mode C, the MODE C LED will be illuminated. The CHANNEL switch selects which channel is being calibrated. Bit 8 of the BIT TABLE switch controls the direction the offset increments. Bit 7 of the BIT TABLE controls the increment step size. The calibration value will wrap over when the maximum or minimum value is reached.

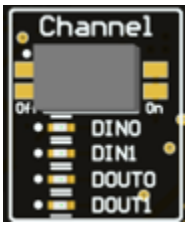
Pressing the BUTTON starts or stops the incrementing calibration for the currently selected channel. When the button is pressed to stop the calibration, the current calibration value is written to non-volatile memory, indicated by three blinks on the STATE Memory LED.

Mode D

Unused: MODE D is not implemented.

Channel

The channel switch, located in the Channel box, selects which channel is being controlled. A bit is set low when the switch is toggled to the left side and set high when toggled to the right side.



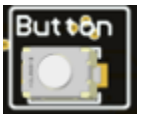
Channel Switch		
Bits	**Value**	**Setting**
[1 : 0]	00 (0)	DIN0
	01 (1)	DIN1
	10 (2)	DOUT0
	11 (3)	DOUT1

☞ If the board is in MODE A, the channel switch is ignored, and all four channels are selected (broadcast mode).

State

When illuminated, the two state LEDs, Memory and Switch, indicate whether the amplifier is using settings from the non-volatile memory or BIT TABLE switches. On power-up the board will automatically use settings from non-volatile memory, refer to MODE A and MODE B for more details.

Button



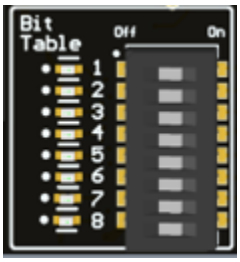
The button is not typically used in MODE A or MODE B. The button is used to start and stop the OFFSET CANCELLATION FIELD CALIBRATION PROCEDURE.

☞ If the button is pressed and held for approximately five seconds, this will erase any user-saved values, depending on Mode. If you are in MODE A or MODE B default bit table settings will be applied. If you are in MODE C factory-default offset calibrations values will be applied.

Bit Table

The bit table switches are used to set amplifier settings and control offset calibration. Refer to the tables below for a description of the controls. The LEDs represent the settings that are currently applied to the amplifier channels. When a BIT TABLE value is changed, the new settings are applied and programmed to non-volatile memory as defined by the selection. The Memory LED will blink three times, indicating new switch value was written to non-volatile memory.

Bit Table Settings – Mode A and B		
Bit	**On**	**Off**
8 (TX Override)	Disabled	Enabled (Recommended)
7 (Voltage Overdrive)	-1.6 dB	0 dB (Recommended)
CTLE Bandwidth Control		
Bit	**Value**	**Setting**
[6 : 5]	00 (0)	Lowest
	01 (1)	Low
	10 (2)	Medium (Recommended)
	11 (3)	Highest
CTLE Boost at 8 GHz		
Bit	**Value**	**Setting**
[4 : 1]	0000 (0)	-0.8
	0001 (1)	1.3 (Default)
	0010 (2)	5.7
	0011 (3)	7.1
	0100 (4)	8.4
	0101 (5)	9.1
	0110 (6)	9.8
	0111 (7)	10.7
	1000 (8)	11.3
	1001 (9)	12.6
	1010 (10)	13.6
	1011 (11)	14.4
	1100 (12)	15
	1101 (13)	15.9
	1110 (14)	16.5
	1111 (15)	17.8
0	Unused	Unused



Bit Table Setting – Mode C (Offset Calibration)		
Bit	**On**	**Off**
8 (Increment Direction)	Increase	Decrease
7 (Increment Step Size)	Small	Large
[6:0]	Unused	Unused

Recording Traffic

You can use the Instrument Status counters in the Protocol Insight software to adjust the grypper interposer lane amplifier settings. You can also use the Smart Tune™ equalization settings to further optimize the lanes. After the Falcon G500C/G550C Analyzer and FG5AMPGR Grypper Interposer are properly set up you can capture traces. Refer to the Falcon G500C/G550C User Manual for more information.

Measuring VCC, VCCQ and VCCQ2

The FG5AMPGR interposer board has sense resistors for the VCC, VCCQ and VCCQ2 power supplies, shown in FIGURE 7. Measure the current by using a current probe, such as the Keysight N2820. Remove the sense resistors from the board and replace them with new resistors, with resistance values selected based on the estimated current you will be measuring. Each resistor pad has a “T” and “B” label, which denotes the current flow direction from top (T) to bottom (B).

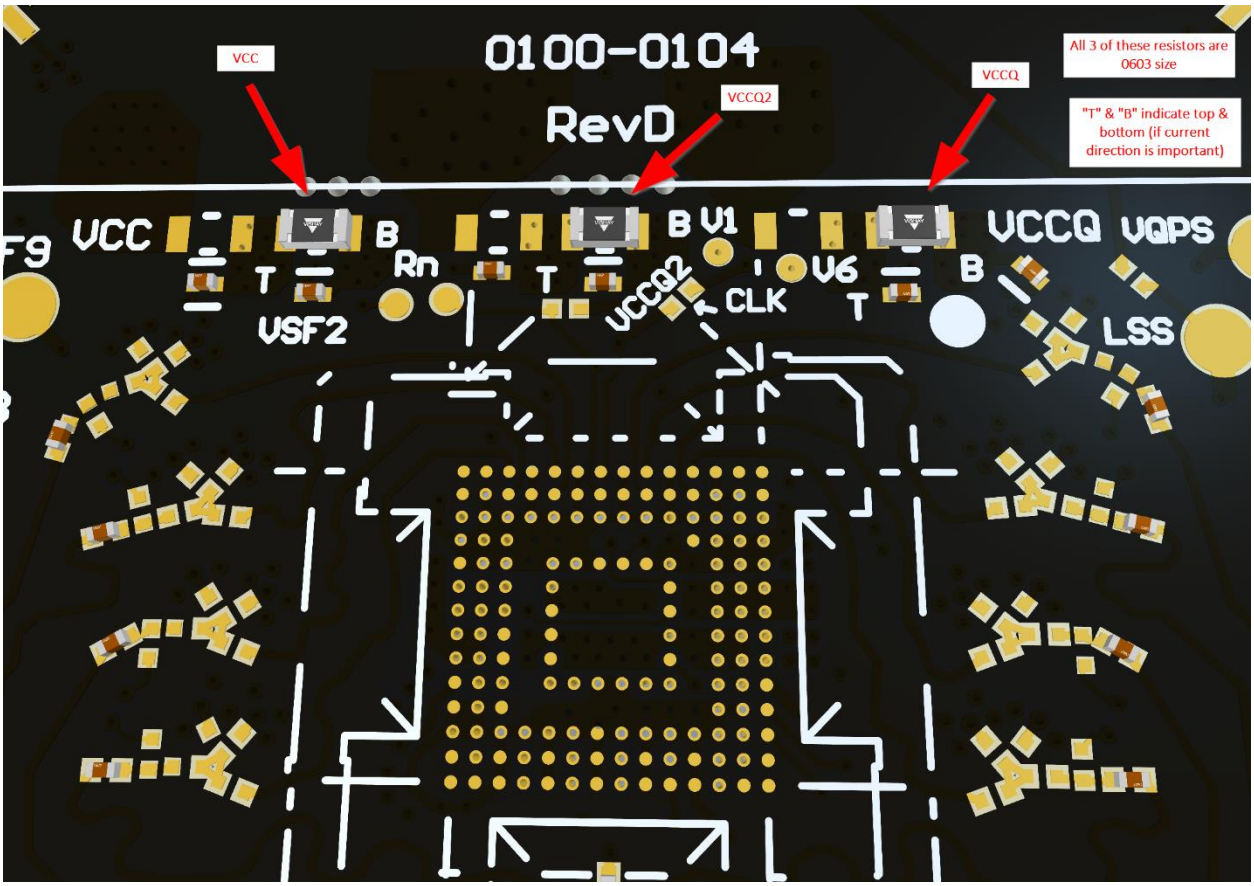


Figure 7 - Sense Resistor Location

Maintenance – Offset Cancellation

Lane offset is defined as the voltage difference between the P & N sides of one differential lane. Ideally there would be no DC offset between these signals. However, there are non-idealities that contribute to DC offset on the lane. This DC offset is unwanted as it contributes to reduced differential signal swing, thus reducing eye height.

The FG5AMPGR is factory calibrated to null the offset voltage between the DOUT and DIN pairs. There are environmental factors, such as ambient temperature, that can cause the offset to drift during use. It is important to occasionally verify that the offset voltage is still within tolerance. The OFFSET CANCELLATION VERIFICATION PROCEDURE explains how to verify the DC offset is acceptable.

Offset Cancellation Verification Procedure

1. ⚠ We recommend contacting Protocol Insight at support@protocolinsight.com before attempting this procedure.
2. Disconnect all inputs and outputs on the FG5AMPGR.
3. Power on the FG5AMPGR and allow it to reach steady state temperature. At least 15 minutes is recommended.
4. ⚠ CAUTION: Do not probe the SMP-mini center pin with DVM test leads as this can damage the center pin. We recommend using SMP-mini cables and adapters to get to DVM banana jacks. A SMP-mini cable can been modified to expose the center coax of the cable, allowing a DVM cable to be clipped to the center coax. Connect the digital voltage multimeter (DVM or DMM) to the P & N SMP-mini ports of the DOUT outputs.
5. Record the DVM results in the table below.

Lane	Offset Value	Lane	Offset Value
DOUT0		DIN0	
DOUT1		DIN1	

6. Repeat steps 3 and 4 for the DIN outputs.
7. If the absolute value of the measured offset voltage for either DOUT or DIN is greater than 3mV, please contact Protocol Insight technical support, refer to CONTACT INFORMATION. The support team may direct you to follow the OFFSET CANCELLATION FIELD CALIBRATION PROCEDURE.

Offset Cancellation Field Calibration Procedure

When in MODE C, **Offset Calibration Mode**, the CHANNEL switch controls which channel is being calibrated. Refer to the CHANNEL section of the document.

1. Disconnect the interposer from any DUT. Disconnect all SMPM outputs. Remove the device.
2. Connect the DMM (digital multimeter) to the first channel to be calibrated, likely DIN0. Set the channel using the CHANNEL switch controls. The polarity of the DMM and lanes does not matter. Note that the direction of the offset correction may appear to be reversed (may step more negatively) depending on DMM connections. Ultimately, the direction does not matter as the goal is to hit zero. Use the same technique described in Item #3 in the OFFSET CANCELLATION VERIFICATION PROCEDURE.
3. Power on the FG5AMPGR and allow it to reach steady state temperature. At least 15 minutes is recommended.
4. Set the Mode select to MODE C, the Mode C LED will be illuminated, confirming you are in this mode.
5. Pressing Button starts changing the offset adjustment based on the BIT TABLE Mode C settings, refer to the BIT TABLE section. The Status LED will illuminate blue, indicating the offset calibration is incrementing.
6. As it approaches 0, toggle BIT TABLE Bit 7 to move into slow mode.
7. When the DMM reading is less than 0.1mV, press the BUTTON again. The STATUS LED will illuminate green, indicating the offset calibration has completed and the values will be written into non-volatile memory.
8. Move the DMM SMPM cables to the next lane to be calibrated and switch to the next channel. Repeat steps 5 through 7 until all lanes have been calibrated.
9. Once all lanes have been calibrated, unplug the power cable and reinsert it.
10. Follow the OFFSET CANCELLATION VERIFICATION PROCEDURE to verify the offset voltages are within specification.

Board Dimensions

FIGURE 8 is a gerber diagram of the board illustrating the dimensions of the FG5AMPGR board. As was shown in FIGURE 1, the interposer board is outlined in yellow and the power board is outlined in orange.

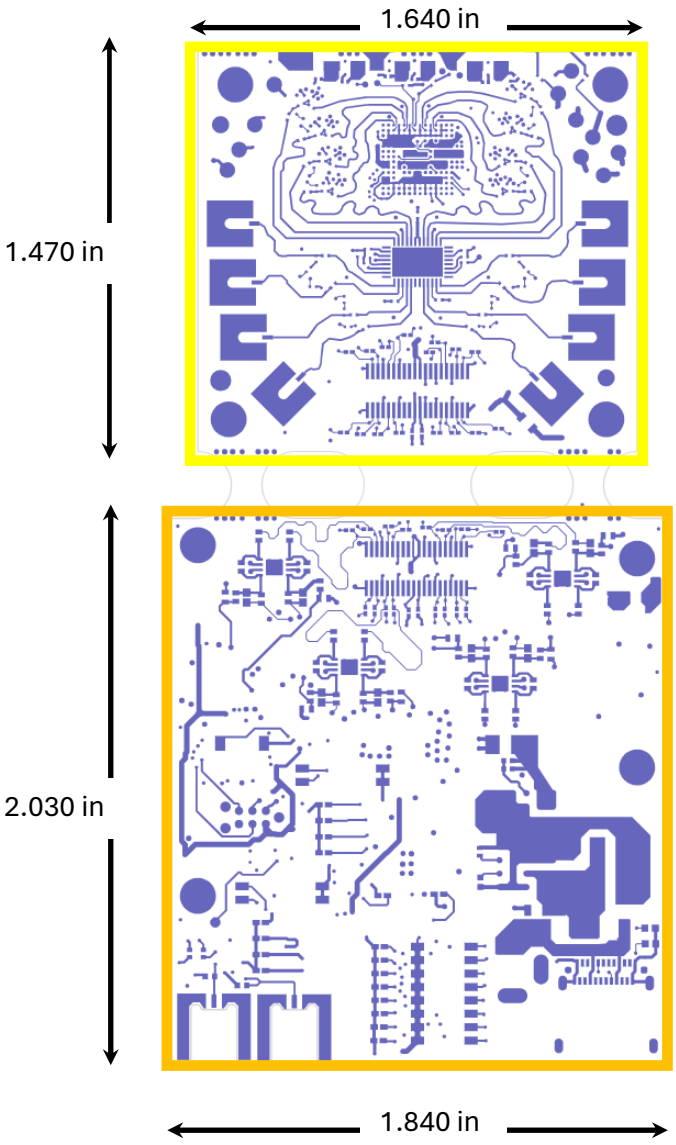


Figure 8 - Board Dimensions

Phase-Matched Cables

The FG5AMPGR may be purchased with the FG5AMPSP-C12 phase-matched cables. These are 12-inch right-angle SMPm to straight SMP cables with low loss and phase matching ≤ 0.5ps, refer to FIGURE 9. The following tables summarize the cable specifications.

Electrical		
Item	**Test Condition**	**Specification**
Impedance	DC – 40 GHz	50 ohms
Voltage Standing Wave Ratio	DC – 40 GHz	1.8 Max
Insertion Loss	DC – 40 GHz	Refer to FIGURE 9
Velocity of Propagation	DC – 40 GHz	76% (nominal)
Working Voltage	AC time 60 sec	150 Vrms Max
Mechanical		
Item		**Specification**
Nominal Outer Diameter		2.33 mm
Min Bend Radius Static		11.7 mm
Min Bend Radius Dynamic		23.3 mm
Temperature Range		-55 – 125 C

Figure 9 - Cable Loss Over Frequency

Interposer "Chiclet" Adapter

In the layer stack-up example, shown in FIGURE 4, the interposer connects to your system with a grypper socket. You can also use "chiclet" adapter cards, which are standard PCB boards with high performance SAMTEC ADF6 connectors. Two adapters are used to attach the interposer to your system. The adapters solder to the system board and the interposer card (balls shown in green), this is shown in FIGURE 10. A future revision of the interposer will use the SAMTEC connector directly, only a single adapter card will be required for the system board.

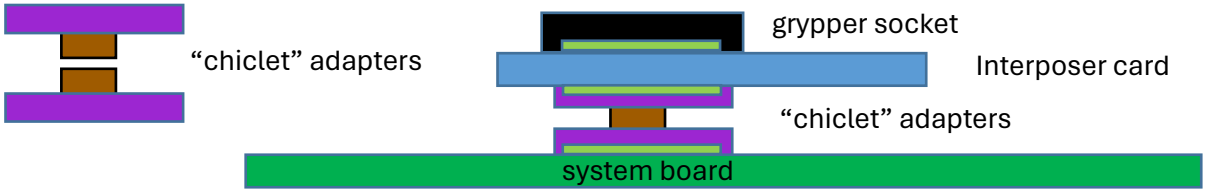


Figure 10 - Layer Stack-Up with "chiclet" Adapters

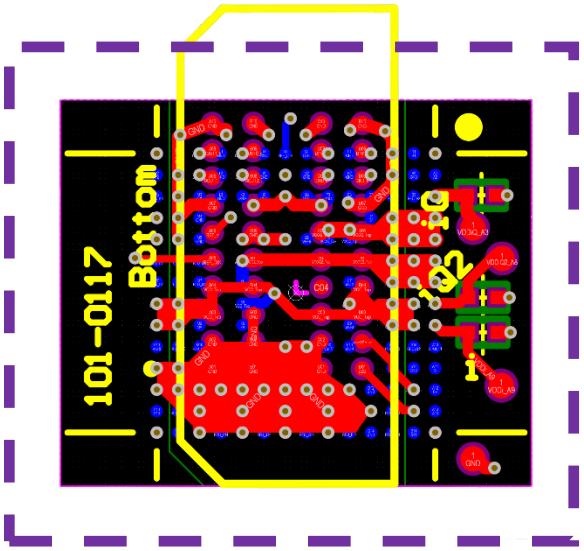


Figure 11 - "chiclet" Connector Layout

The PCB board for the "chiclet" adapter, 9 x 11mm in the black outline, is shown in FIGURE 12. The outer dashed purple line is the standard UFS package size, 11.5 x 13 mm, and is shown for reference. The SAMTEC connector, rectangle shown in yellow, was intentionally placed to optimize signal integrity for the 24 Gpbs M-PHY signals and overhangs the PCB by 2.0117 mm. In FIGURE 10, the "chiclet" PCB thickness, shown in purple, is 62 mils (1.57 mm). and the SAMTEC connector is 3.73 mm in height, shown in brown.

The top and bottom side view of the adapter board pair (which separates in the middle) is shown in FIGURE 14 and FIGURE 12, respectively. The passthrough signals are shown in FIGURE 14.

Refer to the Chiclet Guidelines document for information on how to attach the chiclet.

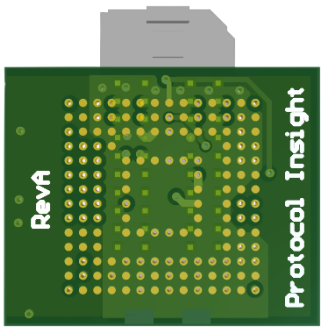


Figure 14 – Ball Array Side View

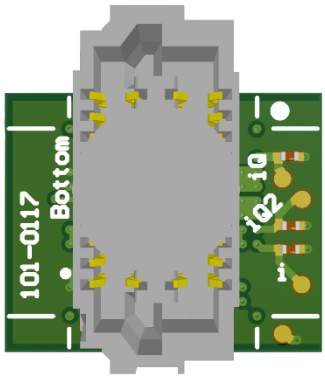


Figure 12 - Connector Side View

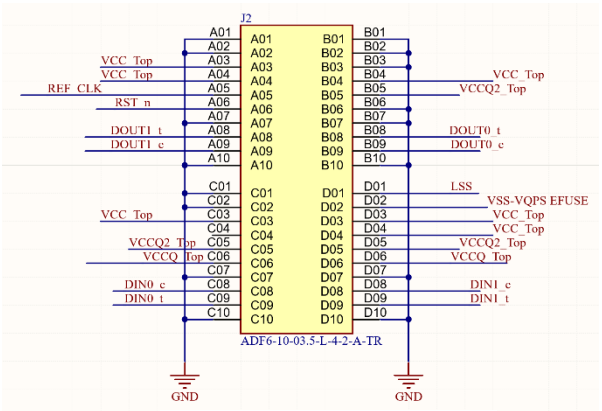


Figure 13 - Schematic Signals

Operating Conditions

The accessory is intended for indoor use and should be operated in a clean, dry environment. Before using this product, ensure that its operating environment is maintained within these parameters:

Temperature: -20C° to 55° C.

Humidity: Operating humidity range 10 to 80%.

Altitude: Up to 10,000 ft (3,048 m).

Contact Information

1. For additional information, to request a demonstration or quote, or place an order, please contact your local Protocol Insight representative or sales@protocolinsight.com
2. Support materials and examples files are available at http://www.protocolinsight.com/support-materials/
3. For technical support please contact your local Protocol Insight representative or support@protocolinsight.com