PROTOCOL INSIGHT

HS-G5 Amp Splitter (FG5AMPSP)

Quick Start / User Guide

Contact Protocol Insight at:

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Introduction

The amp splitter, FG5AMPSP, board allows developers to tap signals between the Host and DUT and send them to a protocol analyzer using SMP-mini connectors.

The amp splitter board uses a 66 / 33 resistive divider and provides the “66” side to the Host / DUT. This provides an additional ~ 2 dB of signal for the Host / DUT, compared to a 50 / 50 resistive divider. The “33” side is then amplified and sent to the protocol analyzer. The amplification settings are adjustable.

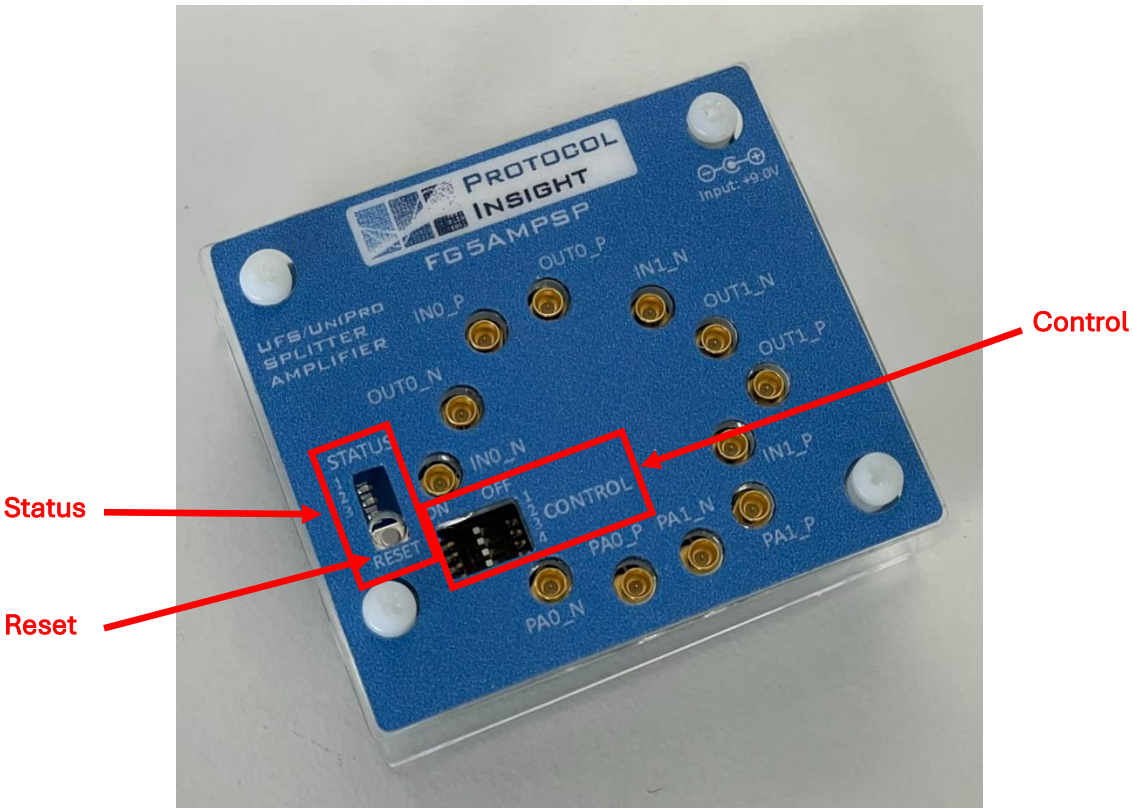


Figure 1 – FG5AMPSP Production Board

Use Case Requirements

The amp splitter requires the following minimum differential signal requirements at a given bit error rate at the SMP connection point. If an oscilloscope is available, you can confirm your test configuration aligns with these parameters.

- Inner eye width = 100ps Minimum for GEAR3, 60ps for GEAR4 and 30ps for GEAR5 (Figure 2).
- Inner eye height = 90 mVpp Minimum (Figure 2)
- Eye Amplitude = 620 mV (Figure 2)
- Maximum differential signal amplitude 620 mVpp (Figure 2)

FIGURE 2 shows the EYE diagram requirements at the probing point for GEAR3, GEAR4, GEAR5 signal rates.

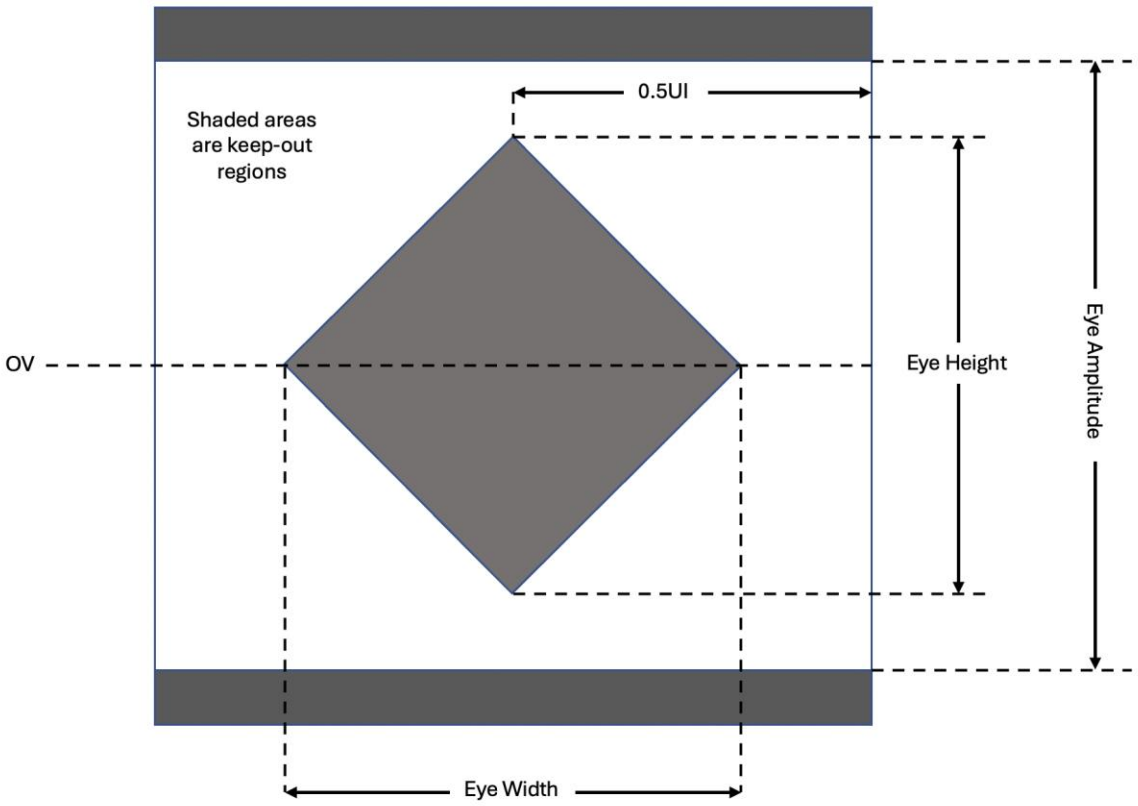


Figure 2 - EYE Diagram

Connecting the Amp Splitter

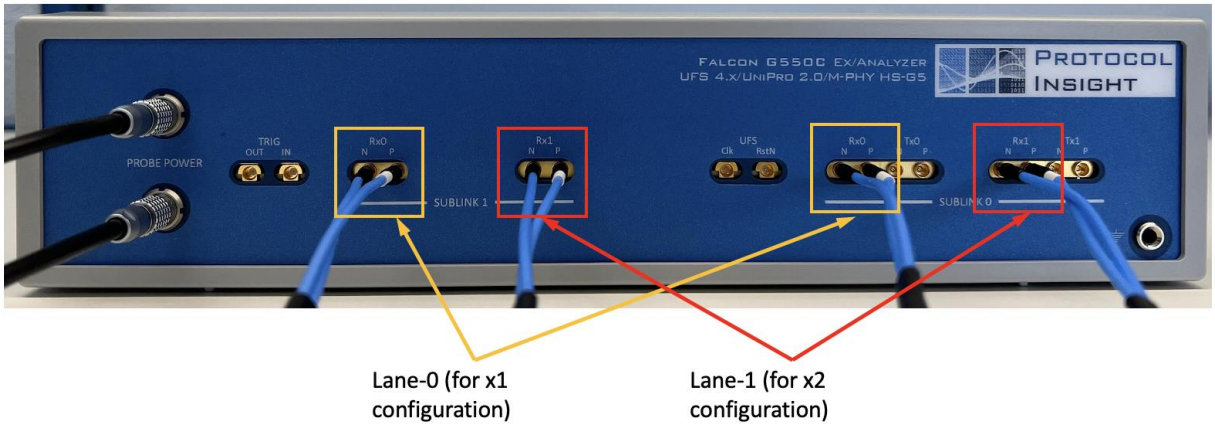


Figure 3 - Cabling Between Amp Splitter and Analyzer

Cable Configuration

When connecting the DUT, ensure you use low-loss, phase matched cables. The connectors on the amp splitter board, FG5AMPSP, are male SMP-mini. The connectors on the protocol analyzer are male SMP. Below are the cable characteristics we recommend:

- Low-loss material, < 1 dB per foot of insertion loss @ 12 GHz.
- Limit the length of the cables to < 12-inches in length.
- The cables must be 50 ohm and phase matched.
- Right angle SMP-mini cable to ease escapement from board.

Match the P/N connections when connecting the cables (P to P, N to N). The recommended cable, FG5AMPSP-C, is a 12-inch phase matched SMP female (protocol analyzer side) to a right angle SMP-mini female (amp splitter side). We strongly recommend using a cable extraction tool to avoid damaging the connectors or cables.

Recommended Connection for a x1 Configuration

In a x1 configuration we expect a host and device single lane configuration. Use two matched pairs of SMP-mini to SMP cables to connect the PA0 and PA1 to the protocol analyzer Sublink 0 Rx0 or Sublink 1 Rx0, respectively. Lane 0 from the host and device must connect to Rx0 on the PA. **Example:** PA0 should connect to Sublink 0 Rx0 and PA1 should connect to Sublink 1 Rx0.

Recommended Connection for a x2 Configuration

In a x2 configuration we expect a host and device dual lane configuration. Use four matched pairs of SMP-mini to SMP cables to connect the PA0 and PA1 from both FG5AMPSP boards to the protocol analyzer, Sublink 0 Rx0 and Rx1 and Sublink 1 Rx0 and Rx1. As previously noted, Lane 0 from the host and device must connect to Rx0 on the PA. Similarly, Lane 1 must connect to Rx1 on the PA and be in the same Sublink as Lane 0. **Example:** PA0 and PA1 on the first FG5AMPSP board should connect to Sublink 0 Rx0 and Rx1, respectively. PA0 and PA1 on the second FG5AMPSP board should connect to Sublink 1 Rx 0 and Rx1, respectively.

Onboard Switch Settings

S1 is a 4-bit maintained switch bank, labeled **Control** in FIGURE 1. These four switches provide binary controls for RF settings in the main amplifier. The LSB of the 4-bit control is labeled **1** in Figure 1. **4** is the MSB. The ON side of the switch is a logic '1'.

The table of controls is shown below.

Switch State	CONTROL (1 is LSB)	CTLE Bandwidth	Mid-band Compensation	Output Differential Voltage Swing (dB)	CTLE Value (dB @ 8GHz)
0	0000	Low	Enabled	0	-0.8
1	0001	Low	Enabled	0	1.3
2	0010	Recommended	Enabled	0	-0.8
3	0011	Recommended	Enabled	0	1.3
4	0100	Recommended	Enabled	0	5.7
5	0101	Recommended	Enabled	0	7.1
6	0110	Recommended	Enabled	0	10.1
7	0111	Recommended	Enabled	0	14.4
8	1000	Recommended	Enabled	0	17.85
9	1001	Recommended	Disabled	0	1.3
10	1010	Recommended	Disabled	0	5.7
11	1011	Recommended	Disabled	0	7.1
12	1100	Recommended	Enabled	-1.6	-0.8
13	1101	Recommended	Enabled	-1.6	1.3
14	1110	Recommended	Enabled	-6	-0.8
15	1111	Recommended	Enabled	-6	1.3

Status Lights

The Amp Splitter has one power LED and three status LEDs on the top side of the daughter board, labeled **Status** in FIGURE 1.

Status lights #1 and #2 are blue lights used to indicate microcontroller modes, these are discussed in the Microcontroller Modes section. Status light #3 is an orange light used to indicate errors. The power LED is located near the DC jack and indicates that the board is powered.

Power-Up

The Amp Splitter board does not have a power switch and powers up when the DC jack is inserted. When power is applied, all three status LEDs will briefly illuminate to indicate the microcontroller is running.

Errors

Status light #3 will briefly illuminate during power-up and will stay lit whenever the microcontroller encounters an error. If Status light #3 is illuminated, you must power cycle the board to clear the error state. *Contact Protocol Insight if Status light #3 continues to illuminate after repeated power resets.*

Microcontroller Modes

Refer to Onboard Switch Settings for more detail on the **Control** bank settings. Below

Mode	Status Lights	Channel
Memory Mode	#1 (on) #2 (on) #3 (off)	Each lane is using the control bank settings written during a previous use.
Broadcast Mode	#1 (off) #2 (off) #3 (off)	Both lanes are set to the same **Control** bank setting.
Channel Mode – Lane 0	#1 (on) #2 (off) #3 (off)	Lane 0 is set based on the **Control** bank setting.
Channel Mode – Lane 1	#1 (off) #2 (on) #3 (off)	Lane 1 is set based on the **Control** bank setting.
Error	#3 (on)	If status light #3 remains lit, power cycle the board. Refer to Errors for more detail.

By default, the microcontroller is in **broadcast mode** and status lights #1 and #2 are not illuminated. In broadcast mode both lanes are set to the same value based on the **Control** bank settings.

Pressing the **Reset** button causes the microcontroller to switch into **channel mode**. In **channel mode**, status light #1 illuminates, indicating Lane0 is selected. The **Control** bank selection sets the value for the Lane0 amplifier channel (IN0_N, IN0_P, PA0_N & PA0_P). Any change to the **Control** bank settings will be applied to Lane0 amplifier channel until the **Reset** button is pressed again.

Pressing the reset button again selects the Lane1 amplifier channel (IN1_N, IN1_P, PA1_N & PA1_P) and status light #2 will be illuminated. Any change to the **Control** bank settings will be applied to the Lane1 amplifier channel until the **Reset** button is pressed again.

When in **channel mode**, the **Control** settings for each selected channel are written to non-volatile memory. If the unit is powered cycled, and both status lights #1 and #2 remain illuminated, you are in **memory mode**. This indicates the microcontroller is using previously saved control bank values for each channel.

When in memory mode, there are two ways to change channel amplifier settings.

Method 1

Pushing the reset button will cause the microcontroller to enter channel mode. The lane settings can be altered by changing the Control settings as previously described.

Method 2

If you hold the Reset button for approximately five seconds, the microcontroller will erase the previously saved channel amplifier settings and go back to broadcast mode. When you reach the mode, the #3 LED will light, followed by #1, #2, and #3 illuminating, indicating that the microcontroller has been reset and is in broadcast mode. The Control will now control both lanes using the current settings on the 4-bit switch as previously described.

Recording Traffic

You can use the Instrument Status counters in the Protocol Insight software to adjust the amp splitter lane amplifier settings. You can also use the Smart Tune™ equalization settings to further optimize the lanes. After the Falcon G500C/G550C Analyzer and FG5AMPSP Amp Splitter are properly set up you can capture traces. Refer to the Falcon G500C/G550C User Manual for more information.

Maintenance – Offset Cancellation

Lane offset is defined as the voltage difference between the P & N sides of one differential lane. Ideally there would be no DC offset between these signals. However, there are non-idealities that contribute to DC offset on the lane. This DC offset is unwanted as it contributes to reduced differential signal swing, thus reducing eye height.

The FG5AMPSP is factory calibrated to null the offset voltage between the PA0 & PA1 pairs. There are environmental factors, such as ambient temperature, that can cause the offset to drift during use. It is important to occasionally verify that the offset voltage is still within tolerance. The Offset Cancellation Procedure explains how to verify the DC offset is acceptable.

Offset Cancellation Procedure

1. We recommend contacting Protocol Insight at support@protocolinsight.com before attempting this procedure.
2. Disconnect all inputs and outputs on the FG5AMPSP.
3. Power on the FG5AMPSP and allow it to reach steady state temperature. At least 15 minutes is recommended.
4. ⚠ **CAUTION:** Do not probe the SMP-mini center pin with DVM test leads as this can damage the center pin. We recommend using SMP-mini cables and adapters to get to DVM banana jacks. Refer to FIGURE 4, a SMP-mini cable has been modified to expose the center coax of the cable, allowing a DVM cable to be clipped to the center coax. Connect the digital voltage multimeter (DVM or DMM) to the P & N SMP-mini ports of the PA0 outputs.
5. Record the DVM results in the table below.

Lane	Offset Value
PA0	
PA1	

6. Repeat steps 3 and 4 for the PA1 output.
7. If the absolute value of the measured offset voltage for either PA0 or PA1 is greater 3mV, please contact Protocol Insight technical support, refer to Contact Information.

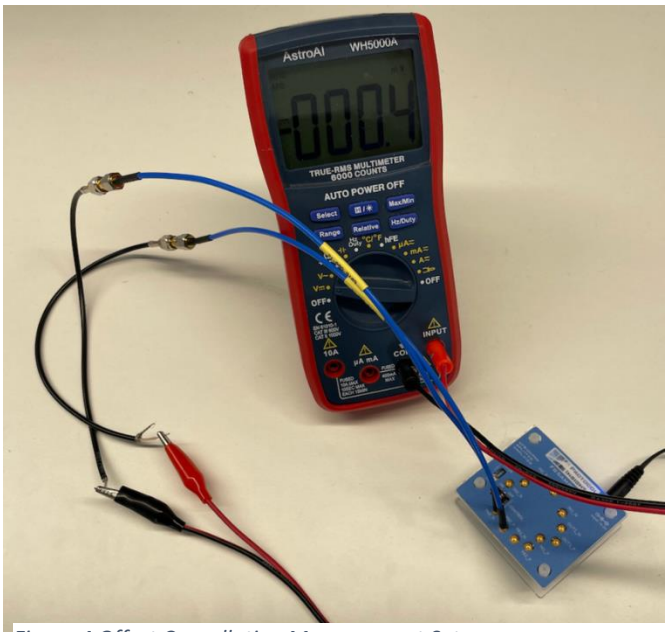
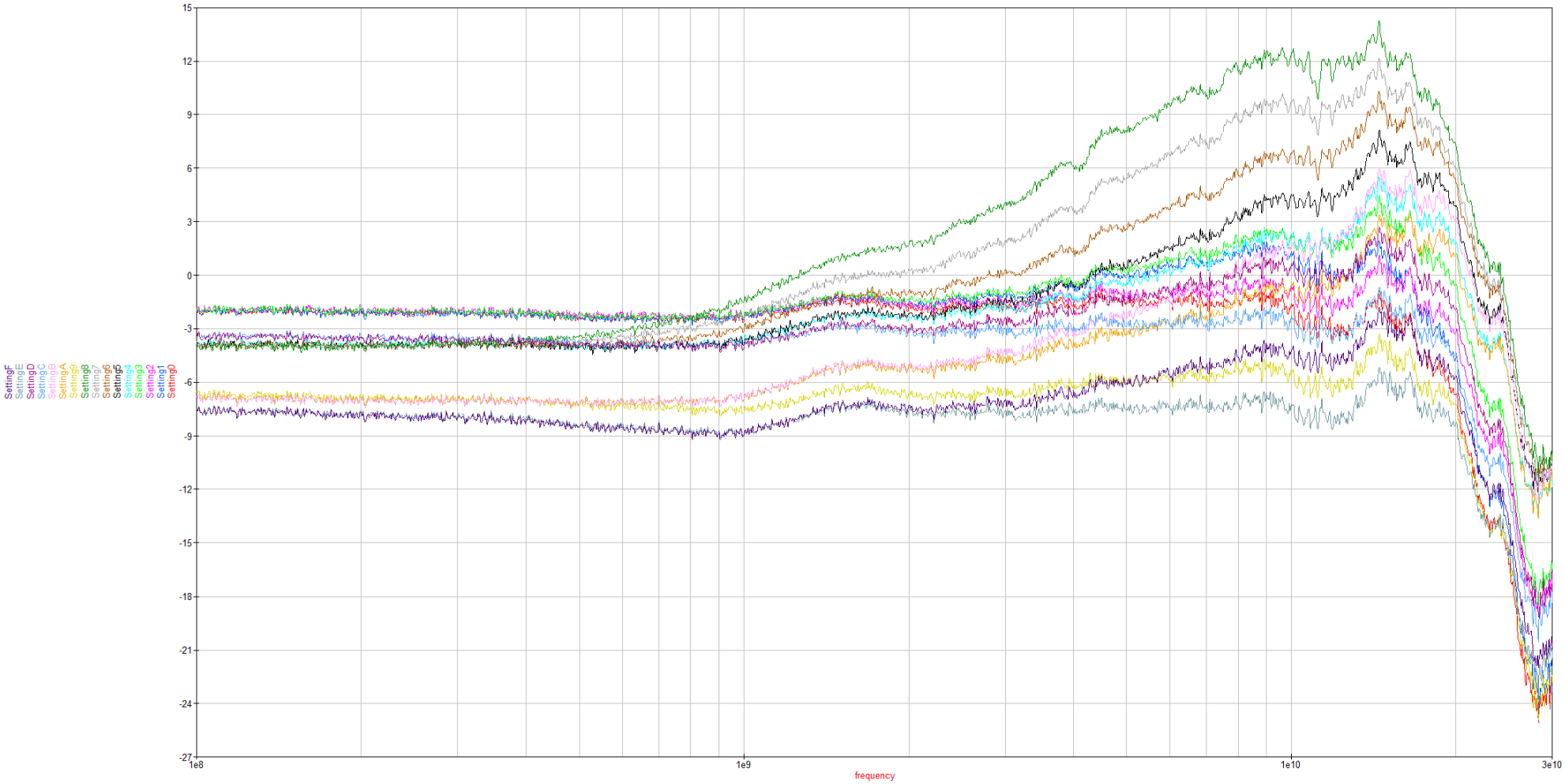
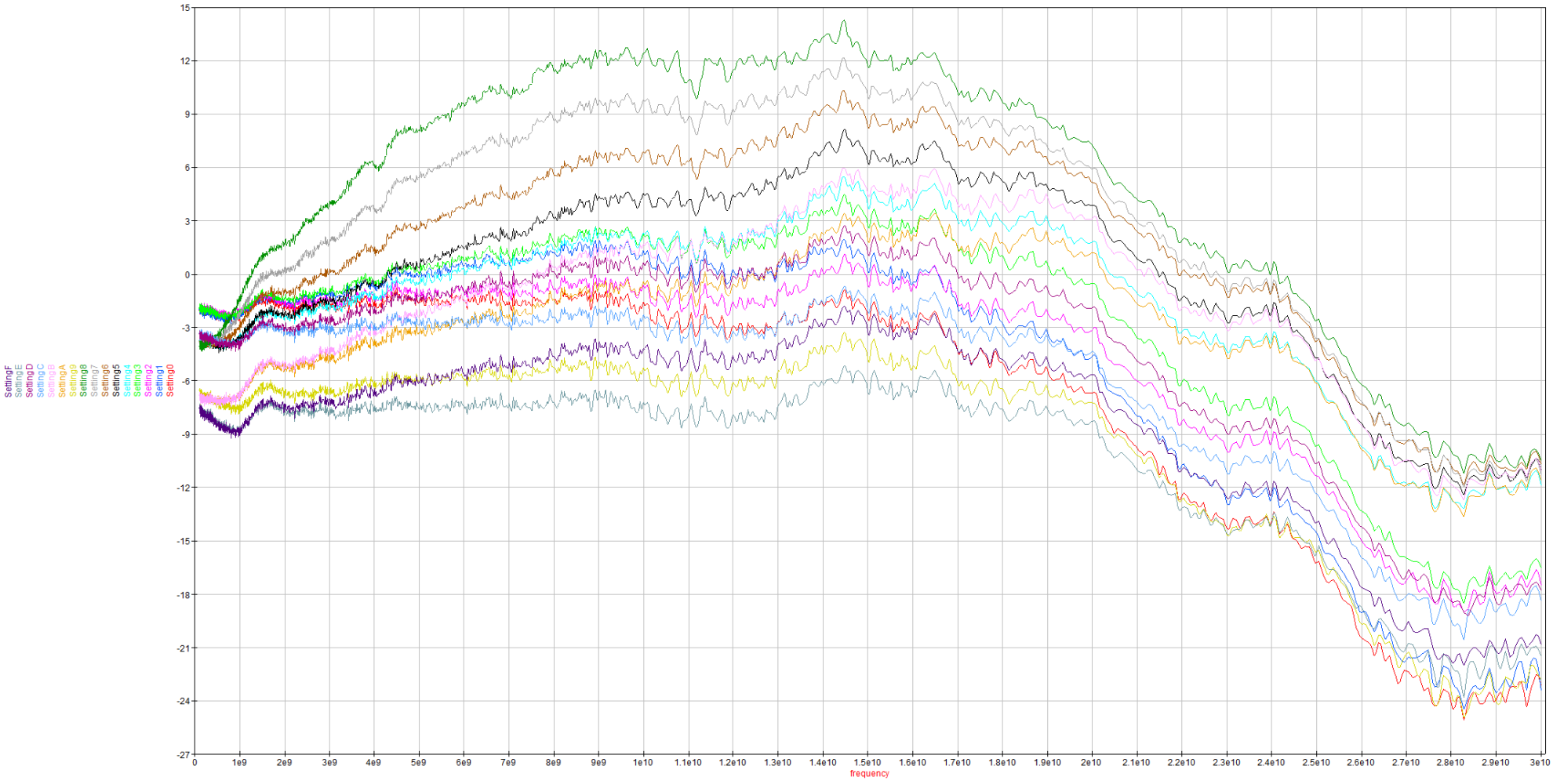


Figure 4 Offset Cancellation Measurement Setup

Switch Setting Frequency Response Log



Switch Setting Frequency Response Linear



Phase-Matched Cables

The FG5AMPSP may be purchased with the FG5AMPSP-C12 phase-matched cables. These are 12-inch right-angle SMPm to straight SMP cables with low loss and phase matching ≤ 0.5ps, refer to Figure 5. The following tables summarize the cable specifications.

Electrical		
Item	**Test Condition**	**Specification**
Impedance	DC – 40 GHz	50 ohms
Voltage Standing Wave Ratio	DC – 40 GHz	1.8 Max
Insertion Loss	DC – 40 GHz	Refer to Figure 5
Velocity of Propagation	DC – 40 GHz	76% (nominal)
Working Voltage	AC time 60 sec	150 Vrms Max
Mechanical		
Item		**Specification**
Nominal Outer Diameter		2.33 mm
Min Bend Radius Static		11.7 mm
Min Bend Radius Dynamic		23.3 mm
Temperature Range		-55 – 125 C

Figure 5 - Cable Loss Over Frequency

Operating Conditions

The accessory is intended for indoor use and should be operated in a clean, dry environment. Before using this product, ensure that its operating environment is maintained within these parameters:

Temperature: 5° to 40° C.

Humidity: Operating humidity range 10 to 80%.

Altitude: Up to 10,000 ft (3,048 m).

Contact Information

1. For additional information, to request a demonstration or quote, or place an order, please contact your local Protocol Insight representative or sales@protocolinsight.com
2. Support materials and examples files are available at http://www.protocolinsight.com/support-materials/
3. For technical support please contact your local Protocol Insight representative or support@protocolinsight.com